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VIB-3 Superconducting versus Optical Interconnections—S. K. Tewksbury, L. A. Hornak and M. Hatamian, AT&T Bell Laboratories, Holmdel, NJ 07733.

High-T_c superconductors, combined with "cold" silicon MOS devices, may provide superior high-speed interconnections within electronic systems [1] for interconnection distances between about 1 cm and a few meters. Optical interconnections, avoiding the need for reduced operating temperatures, are also targeted for this distance range. Our studies on advanced interconnection technologies assume an advanced packaging scheme using wafer-level electronic components. Here, we contrast the results of our work on "long" (30 cm) YBaCuO microstrip interconnections and "short" (< 10 cm) waveguided optical interconnections.

4000-Å YBaCuO films were coevaporated on 1-in square $LaGaO_3$ substrates and a 30-cm microstrip (125-μm-wide line on 375-μm pitch, using a spiraled rectangular layout) was patterned by liftoff.[1] Separate substrates with superconducting signal and ground plane were separated by a 125-μm-thick sapphire spacer. DC resistance of pressure contacts at the ends of the line was less than 1 Ω below 30 K. Two-point dc resistance measurements showed a sharp transition (about 2 K) at T_c = 86 K and a small normal resistance intercept at 0 K. TDR measurements showed the expected small variation in delay below 50 K, with a rapid increase in delay above 60 K. By monitoring changes (due to impedance changes) in the several transmission amplitude response zeroes between dc and 1.2 GHz, several low-frequency performance factors were readily evaluated. Critical current J_c, defined here as the dc current level causing a 1-dB decrease in a small amplitude, 20-MHz fundamental, decreased from 2×10^5 Acm^{-2} at 68 K to 0.3×10^5 Acm^{-2} at 80 K. The transmission amplitude response showed negligible effects of dc currents (up to levels near the critical current) and of externally applied magnetic field (up to 400 G, well above $H_{c1} \approx 100$ G) at temperatures below 76 K. This suggests that flux motion did not induce significant line resistance under those conditions. As the temperature increases above 76 K and approaches T_c, the transmission zeroes are increasingly damped, with the expected large dc attenuation appearing above T_c. These results suggest 1) that flux motion does not introduce significant nonlinearities below 76 K, 2) that J_c rather than H_{c1} is the appropriate limit on maximum current density, and 3) that high-performance transmission lines can be achieved if the low surface resistance expected for superconductors is achieved. In separate measurements at Lincoln Labs[2] on similarly prepared films, the surface resistance of a YBaCuO ground plane used with a niobium resonator at 4.2 K could not be distinguished from that of a niobium ground plane, placing an upper limit on surface resistance about eight times that of niobium.

Optical interconnects are the principle competitor to superconducting transmission lines for very high data rates on wafer-level components. We have recently evaluated an alkyl-silicon polymer waveguide material in which the waveguide is defined simply by exposure to deep UV, requiring no etching or other patterning of the material. Attenuations less than 0.5 dB/cm were measured on 1-cm waveguides and low loss bends (1-mm radius) and single plane crossovers were demonstrated. Spin applied over a planarizing layer, the optical interconnects formed are directly compatible with underlying electronics and optoelectronics and suitable for length up to several cm (limited by attenuation). The major limitation lies in the optoelectronic sources and in the receiver circuitry. Successful development of GaAs-on-silicon would greatly relax this constraint for adding optical interconnects to silicon VLSI wafer-level components.

[1]Films were deposited and patterned by R. E. Howard, P. M. Mankiewich and B. L. Straughn, AT&T Bell Labs. Substrates were grown and prepared by C. D. Brandle, AT&T Bell Labs.

[2]Dan Oakes, MIT/Lincoln Labs.

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VIB-4 Performance of Vertically Coupled Backside Fiber-Optic Interconnects to GaAs—Robert W. Ade and Eric R. Fossum, Center for Telecommunications Research, Columbia University, New York, NY 10027, and Michael A. Tischler, IBM Thomas J. Watson Research Center.

A vertical coupling technique suited for dense fiber-optic interconnection of 2-D device arrays in GaAs has recently been developed; it employs cavities etched in the backside of the wafer to align each fiber to a diaphragm photodetector (DPD) fabricated on the front-surface epitaxial layers. Operation of the fiber-pigtailed DPD's is described below. Enhanced optoelectronic performance due to the backside approach, as well as the capability of addressing interconnect arrays with approximately 10 fibers/mm^2, is reported.

Photodetectors were fabricated on MOVPE-grown epitaxial films consisting of the following layers: a 4-μm $Al_{0.35}Ga_{0.65}As$ stop-etch/window layer, a 1-μm undoped GaAs buffer, and a 0.4-μm GaAs MESFET layer with $N_d = 8 \times 10^{16}$. Metal-semiconductor-metal (MSM) diodes, FET's with direct illumination of the transistor channel, and a Schottky diode/FET amplifier pair were placed on adjacent mesas. Portions of the GaAs substrate were removed after device fabrication by selective CCl_2F_2RIE [1], leaving the detectors on epitaxial diaphragms approximately 125 μm in diameter. The vertical anisotropy of the RIE process reduces the area consumed by each interconnect so that simultaneous pigtailing of adjacent DPD's was readily achieved for devices spaced only 250 μm apart.

Photocurrent crosstalk, arising from steady illumination of an adjacent detector site, was less than −50 dB for DPD's coupled via backside cavities. This figure is lower than for front surface illumination (−20 to −25 dB crosstalk) because of reduced light scattering. An upper bound on crosstalk during pulsed operation was established at −20 dB, the sensitivity limit of the measurement. Rise and fall times for the photodiodes in the present study were determined to be less than 1 ns, which was the response time of the optical source. The FET structure accommodating direct illumination of the transistor channel operated in a photoconductive mode, with a fall time of 5–10 ns and gain-bandwidth product of 1 GHz.

Backside illumination yielded a threefold higher responsivity (0.4 A/W) for MSM diodes with 50-percent metal coverage of the active region. This is due to an elimination of shadowing by metal contacts, an increase in the effective optical thickness (because of reflection from the contacts), and more efficient carrier collection. The net quantum efficiency at 840 nm of the pigtailed Schottky and MSM diodes ranged from 45–60 percent at low bias (< 5 V). Finally, the dark current (1 nA at −5 V) and photoresponse of the DPD's did not show any degradation as a result of the backside RIE process.

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VIB-5 Germanium p-Channel MOSFET's with High Channel Mobility, Transconductance, and *k*-Value—Suzanne C. Martin, Lorin M. Hitt, and James J. Rosenberg, Division of Engineering, Brown University, Providence, RI 02912.

One motivation for studying germanium MOS technology is the fact that the bulk hole mobility in germanium is roughly four times larger than in silicon—which suggests that germanium might be an excellent candidate for high-performance CMOS. Previous studies of p-channel germanium MOSFET's [1], [2] have not, however, demonstrated channel mobilities which are comparably larger than silicon p-channel mobilities. In this study we are reporting p-channel germanium MOSFET's which *do* exhibit channel mobilities more than four times higher than typically obtained in p-channel silicon devices (in excess of 1000 $cm^2/V \cdot s$ with a gate dielectric thickness of ~ 220 Å).

Fabrication of these MOSFET's is quite straightforward and utilizes equipment which is comparable to that used for conventional silicon MOSFET processing. The material which is used as both the gate dielectric and field passivation is a nitrided, thermally grown native oxide which has been described elsewhere [3]. Following a blanket growth of ~ 220-Å nitrided oxide, a blanket arsenic implant of 3×10^{12} cm^{-2} at 50 keV is performed. This provides both a field stop as well as a threshold adjustment implant. This is followed by a deposition of ~ 1200 Å of Ge_3N_4 by LPCVD. Active areas are opened by wet chemical etching (phosphoric acid). Approximately 220 Å of nitrided oxide gate dielectric is grown next. The channel is masked by a double level overhanging resist "dummy gate," and BF_2 implants of 2.5×10^{15} cm^{-2} at 50 keV are made to form the source/drain regions. The "dummy gate" is then used as a lift-off mask for a thick dielectric. The implants are annealed at 550°C for 75 min. Contact holes are opened to the source/drains, and palladium used as a contact metallurgy. The gate and wiring metallization is chromium-gold.

Germanium p-channel MOSFET's having effective channel lengths down to ~ 2.3 μm (2.75-μm gate length) have been fabricated. Using a dielectric capacitance of 2.5×10^{-7} $F \cdot cm^{-2}$ taken from large area devices, a mobility of ~ 1050 $cm^2/V \cdot s$ can be inferred from the slope of the transconductance curve. For the 2.3-μm device, a transconductance of 50 mS/mm at ~ 0.5 V above threshold and a k value of 110 $mS/V \cdot mm$ have been obtained. This performance is significantly better than that of p-channel silicon devices having similar channel length and ~ 220-Å gate dielectric thickness. Our previous and current results on high channel mobility in n-channel Ge MOSFET's will also be presented for comparison.

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VIB-6 Study of Hole Miniband Transport in Ge_xSi_{1-x}/Si Superlattice—R. P. G. Karunasiri, J. S. Park, K. L. Wang, and F. P. Yuh, Device Research Laboratory, 7619 Boelter Hall, Department of Electrical Engineering, University of California, Los Angeles, CA 90024.

The strained-layer Ge_xSi_{1-x}/Si superlattices and heterostructure have created a great interest due to their potentials in integration with the conventional silicon VLSI technology. In this abstract, we report the first observation of hole-miniband transport in symmetrically strained Ge_xSi_{1-x}/Si superlattices.

Two different kinds of superlattice samples are grown and fabricated. The first kind of samples consists of a single superlattice layer grown on an unstrained $Ge_{x/2}Si_{1-x/2}$/Si buffer layer. A typical structure for this sample consists of p-doped $Ge_{0.4}Si_{0.6}$/Si superlattice (15 periods 50-Å thick for each layer) grown on a p^+ $Ge_{0.2}Si_{0.8}$ buffer layer, and a 7000-Å-thick p^+ $Ge_{0.2}Si_{0.8}$ cap layer on the superlattice for ohmic contact. Two light-hole minibands are expected in this sample from the effective mass calculation. Due to the strain symmetrization, as many superlattice periods as desired can be grown in this structure without suffering the limitation of the critical thickness [1].

The other kind of samples are called band aligned superlattice (BAS) [2] which consist of two superlattices having different minibands. The first superlattice consists of a p-doped $Ge_{0.4}Si_{0.6}$/Si superlattice having 30 periods with 60-Å $Ge_{0.4}Si_{0.6}$ wells, and 40-Å Si barriers grown on a p^+ $Ge_{0.2}Si_{0.8}$ buffer layer. The second superlattice consists of undoped 15 periods of $Ge_{0.4}Si_{0.6}$/Si layers, which has narrower 15-Å $Ge_{0.4}Si_{0.6}$ wells and 30-Å Si barriers. The entire structure is caped with a 7000-Å-thick p^+ $Ge_{0.2}Si_{0.8}$ cap. There are two minibands formed in the first superlattice region and only one miniband in the second superlattice. The miniband of the later superlattice is designed to align with the upper miniband of the first superlattice. Thus, miniband discontinuity is made for the lower miniband in first superlattice.

Mesa diodes of 50–100 μm in diameter are fabricated for electrical measurement. For the simple superlattice sample, current–voltage (I–V) characteristics for forward and reverse biases are almost symmetric. Two peaks are observed from I–V and conductance-voltage (G–V) measurements. Below 100 K, the first peak at near 1 V is clearly observed from the G–V curve, and the second peak at higher voltage (near 2.5 V) shows a clear differential negative resistance (NDR) region. Those peaks are due to the conduction of holes through aligned minibands in the superlattices. The energies of minibands are estimated by thermionic emission analysis of current–voltage–temperature (I–V–T) measurement. For a typical structure the measured energies of the first and second minibands are 95 and 250 meV, respectively. These measured miniband energies are in good agreement with the calculated values.

For the BAS sample, an asymmetric I–V characteristics similar to a p-n junction is observed. Under forward bias, two peaks in the G–V curve at 1 and 2.5 V (at 77 K) are observed. While the reverse bias shows only negligible current up to 3 V. Beyond that the current rapidly increases. The I–V characteristics are due to the alignment of the minibands with the Fermi level at the contact.

The results from our experiments show the clear miniband transport in the Ge_xSi_{1-x}/Si superlattice and further suggests the use of Ge_xSi_{1-x}/Si superlattices for the device applications in infrared detectors and infrared sources using optical transitions between minibands [1].

This work is supported in part by Semiconductor Research Corporation, the Office of Naval Research, and Army Research Office.

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VIB-7 3-D Effects in Emitter–Base Junctions in Advanced Silicon Bipolar Transistors—W. J. M. J. Josquin, J. van Dijk, G. A. M. Hurkx and M. P. G. Knuvers, Philips Research Laboratories, Eindhoven, The Netherlands.

The perimeter of the emitter–base junction is a key factor in the control of self-aligned n-p-n transistors, since it determines not only the emitter–collector punchthrough phenomena but also the emitter–base tunneling and degradation effects. In recent years many papers [1], [2] have analyzed these phenomena in terms of the two-dimensional doping profiles under the oxide spacer which separates the extrinsic base and emitter diffusions.

This paper is the first report on experimental results on double-polysilicon self-aligned n-p-n transistors that clearly indicates that the emitter–base reverse characteristics are inherently limited by