A 15-ns CMOS 64K RAM

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Abstract—**This paper describes a 64K CMOS RAM with an access time of 15 ns. The RAM was built using a technology with self-aligned $TiSi_2$, single-level metal, an average minimum feature size of 1.35 μm, and a minimum effective channel length of 1.1 μm. An access of 10 ns is possible with the word line stitched on a second level of metal and some minor redesign. High speed is achieved through innovative circuits and design concepts. New CMOS circuits include a sense-amp set signal generator, a row decoder, and an input circuit. These circuits feature use of CMOS devices to an advantage for high-speed safe operation. A layout-rule-independent graphics tool was used for the artwork design.**

I. INTRODUCTION

THE DRAMATIC reduction that is taking place in memory access time can be clearly seen in the plot of access time versus year for SRAM's presented at the ISSCC [1]–[16] shown in Fig. 1. FET memories at high levels of integration have moved into the very high-performance area. This downward trend in access time should continue into the foreseeable future. At the 1984 ISSCC we presented a 20-ns 64K NMOS design [5]. Also included on the plot is a 0.78× scaling of that design presented at the 1985 International Symposium on VLSI Technology, Systems, and Applications which gave access times as fast as 11 ns [10]. In this paper we will describe a 64K CMOS RAM with measured access times of under 15 ns and simulated access times of 10 ns with the addition of a second level of metal and some minor redesign.

The characteristics of the 64K CMOS RAM are given in Table I. The high speed of this CMOS RAM is due to a combination of technology and innovative CMOS peripheral circuitry. After a brief description of the technology, three of the key circuits will be described: the sense-amplifier set generator, the row decoder, and the input circuit. In each case, the advantageous use of CMOS devices for high speed while maintaining low-power safe operation will be featured. In addition, the use of this chip to demonstrate a layout-rule-independent physical design tool will be discussed. The use of a high-performance memory chip as a test vehicle served as a challenging demonstration of the potential of the tool.

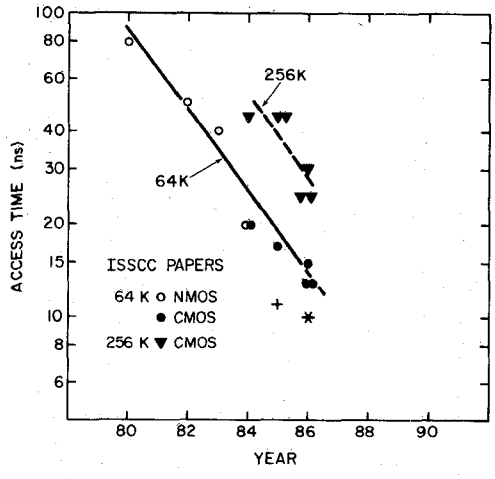

Fig. 1. Plot of access time versus year for SRAM's presented at the ISSCC.

TABLE I
64K CMOS RAM CHARACTERISTICS

Organization	64K (4K x 16)
Cell Type/Area	4-D *NMOS*/210μm^2
Access Time	15ns
Cycle Time	≤ 1.5 T_{ACC}
Supply	5V

II. TECHNOLOGY

The RAM was built using a relatively straightforward CMOS technology with only a single level of metal [17]. Process parameters are given in Table II. A cross section

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TABLE II
CMOS TECHNOLOGY

- Single level metal
- Self-Aligned $TiSi_2$ (5 Ω's/□) over polysilicon and n and p diffusions.
- 22.5 nm gate insulator thickness
- 1.1 μm and 1.2 μm L_{eff} for n- and p-channel devices respectively
- 1.35 μm average minimum feature size
- Junction depth 0.25 μm for n-channel device and 0.30 μm for p channel device.

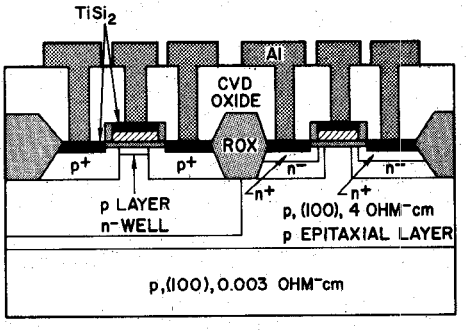


Fig. 2. Cross section of the CMOS structure (from [17]).

of the CMOS structure is shown in Fig. 2. The main features of the technology include:

1) a 1-MeV ion-implanted retrograde n-well;
2) arsenic–phosphorous double diffused n^+/n^- junctions for the n-channel devices to improve the drain breakdown voltage and hot-electron reliability;
3) a self-aligned TiS_2 process with a nitride spacer to reduce the sheet resistances of both polysilicon gates and diffusions; and
4) a 4-μm-thick p-type epitaxial layer grown on a very heavily doped substrate to increase latch-up immunity.

The cell array for this chip was taken from a previous 64K NMOS design (see [5] for a cell layout drawing). It is a four-device cell to which resistors could be added on a second level of poly. The addition of resistors would make the cell fully static and would require no change in the physical or electrical design of the four-device portion of the cell. Thus the RAM performance would be unaffected by the addition of load resistors to the cell. The cell stability and soft error rate with and without load resistors were simulated using conservative assumptions and an analysis methodology that includes transient effects which are important whether dynamic storage or high-resistance loads are used [18]. The cell stability and soft error rate were found to be adequate for several important system applications without the addition of cell load resistors.

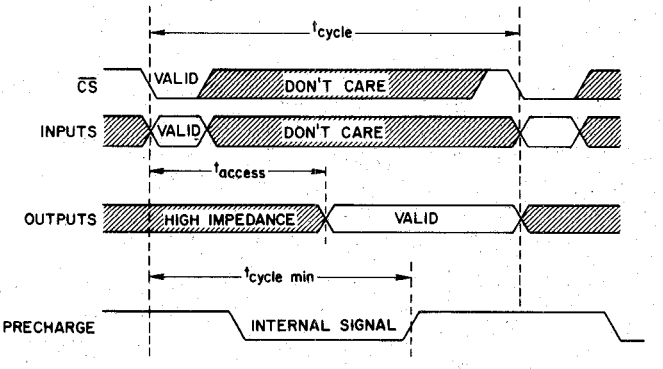


Fig. 3. Waveforms showing 64K CMOS RAM operation.

III. CHIP OPERATION

Chip operation, as shown in the waveforms of Fig. 3, differs from the more conventional approaches which use address-transition detection to initiate the timing chain. In this design a cycle is initiated only by $\overline{CS}$ falling. The inputs are sampled for a short period of time, then all inputs, including $\overline{CS}$, are disconnected until output data have become valid and the precharge of the chip has begun. A longer than minimum cycle is shown. For a minimum cycle, inputs would have to be valid when the precharge of the chip has begun and a new cycle is initiated, as indicated on the figure. The approach offers a number of advantages, listed below, that typically are not available with more conventional approaches.

1) The chip can be operated at minimum cycle time since inputs may be changed during an access.
2) The chip is insensitive to glitches on the inputs once the short sampling period at the beginning of a cycle ends and the inputs are disconnected from the internal chip circuitry.
3) Data outputs are always latched in a valid state or are in a high-impedance state, except when they are in transition.
4) Precharging of internal nodes is automatically initiated at the end of an access.
5) The chip has the same cycle time for any combination of READ and WRITE operations even if data-in and data-out pins are shared.

IV. KEY CIRCUITS

The development of new CMOS peripheral circuitry was key to the high-speed access which was a major objective of the 64K CMOS RAM design. Fig. 4 shows a simplified block diagram of the access path, with the delay through each block indicated. In most of the access path, data simply ripple from block to block, with one block activating the next one. Care was taken to achieve a uniform distribution of delay throughout the critical path. Three of the more important new circuits developed for this design will be described: the self-timed array and sense-amplifier circuitry; the row decoder which uses an innovative two-stage NOR and NAND decoder, and the address buffer

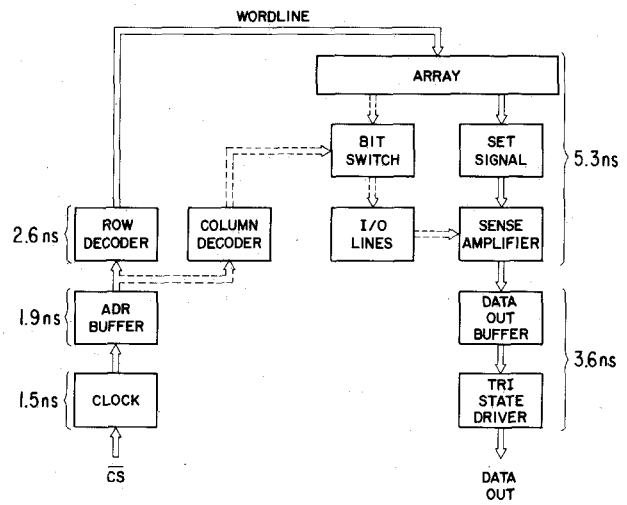


Fig. 4. Simplified block diagram and delay of the 64K CMOS access path.

which uses a nonlinear front end and a self-referencing CMOS latch.

A. Sense-Amplifier Circuitry

The sense amplifier has several unique features including:

a) a sense-amplifier setting waveform that has two distinct slopes for a slow and fast set;
b) a technique for generating the setting signal so it is timed for the accessed word line using p- and n-channel devices; and
c) p-channel decoupling devices between the sense amplifier and the I/O lines for faster setting.

The unique features of the sense-amplifier design result in both very high performance and reliable operation over wide parameter variations. This has been confirmed by simulations and actual hardware results.

The array and sense-amplifier circuitry are shown in Fig. 5. During a READ or WRITE operation, a row and a column decoder will be selected. The selected row decoder will cause its associated word line to go high and the selected column decoder will turn on the gates of the n and p complementary parallel bit-switch devices. The use of dual bit switches is necessary to avoid threshold drops in propagating the cell signal from the bit lines to the I/O lines during a READ or in propagating the signal in the reverse direction during a WRITE. Since the bit lines and I/O lines are high at the start of a READ cycle, the p-channel device forms the best path for conducting the signal. When an I/O line is set to a low level during a WRITE, the n-channel bit switch provides the best path for discharging the bit line to a good low level.

At the end of each word line is the sense-amp set signal generator circuit. As the selected word line rises, it turns on all the memory cells along its length and its set signal generator. A differential voltage builds up across the bit-line pairs as a result of the memory cells turning on. On one of the bit lines the differential voltage propagates

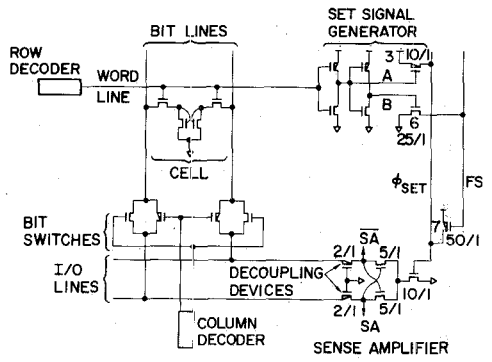


Fig. 5. Array and self-timed sense-amplifier circuitry.

through the selected bit switch onto the I/O lines and sense amplifier. As adequate voltage across the sense-amplifier nodes develops, the fast and slow signal from the set signal generator causes the sense amplifier to latch.

The set signal generator of Fig. 5 is connected both to the ϕ_{SET} line and the *FS* line. Prior to a word line rising, the ϕ_{SET} line is precharged low and the *FS* line is precharged high. As the word line rises, the output (node *A*) of the first inverter stage of the set signal generator falls. Node *A* falling turns on the 10/1 p-channel device 3, which causes ϕ_{SET} to rise in its slow set mode of operation. A short time later the output (node *B*) of the second stage of the set signal generator will rise, causing n-channel device 6 to turn on, which in turn discharges the *FS* line to a low level. Device 7 (a large 50/1 p-channel device) connects the *FS* and ϕ_{SET} lines. When the *FS* line discharges, device 7 turns on and causes ϕ_{SET} to rise in its fast set mode of operation. The slow and fast set slopes and the delays between them can be adjusted by changing the sizes of the devices in the set signal generator and device 7.

In addition to the slow and fast set signal and self-timing from the accessed word line, high-speed operation is further improved by the small p-channel decoupling devices between the small capacitance nodes of the sense amplifier (*SA* and *SAN*) and the high capacitance I/O lines. These decoupling devices make it possible to set the sense amplifier much faster for the same differential signal compared to a sense amplifier without decoupling devices. The *SA* and *SAN* nodes are directly connected to the data-out buffer for further amplification before the signal is driven off-chip.

Simulated sense-amplifier waveforms are given in Fig. 6. The two distinct slopes of the ϕ_{SET} signal can be clearly seen. The smooth transition in slope from slow to fast occurs in conjunction with the increased differential voltage build-up across the sense-amplifier nodes. It can also be seen that the small p-channel decoupling devices make it possible to set the sense amplifier as ϕ_{SET} rises without having to discharge the large bit-line or I/O line capacitances.

Extensive simulations have demonstrated that the design of the set signal generator results in reliable performance even if there are substantial parameter variations. Since the set signal is generated from the selected word line, sensitiv-

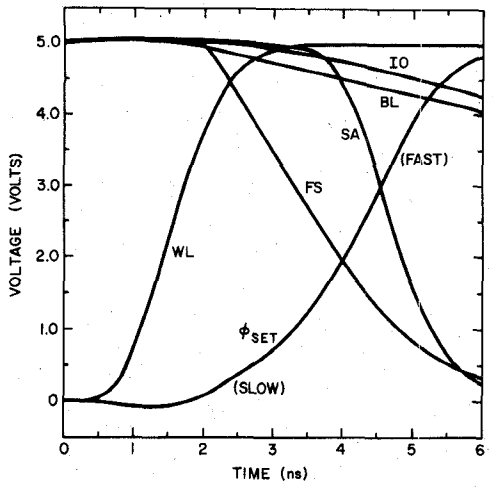


Fig. 6. Simulated sense-amplifier waveforms assuming the use of a second level of metal to stitch the word line.

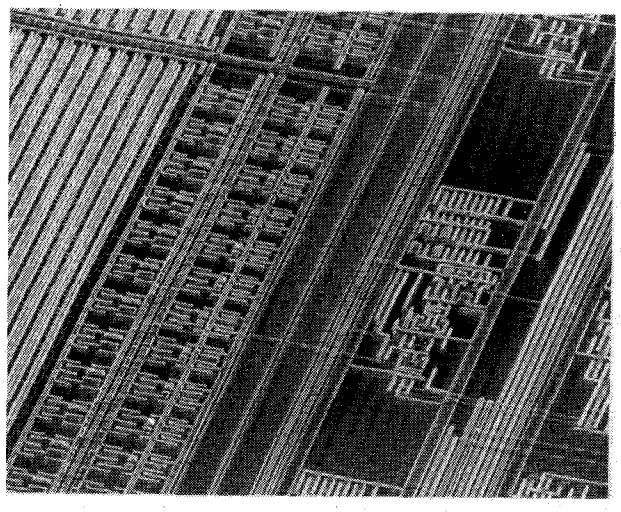


Fig. 7. SEM of array and sense-amplifier circuitry.

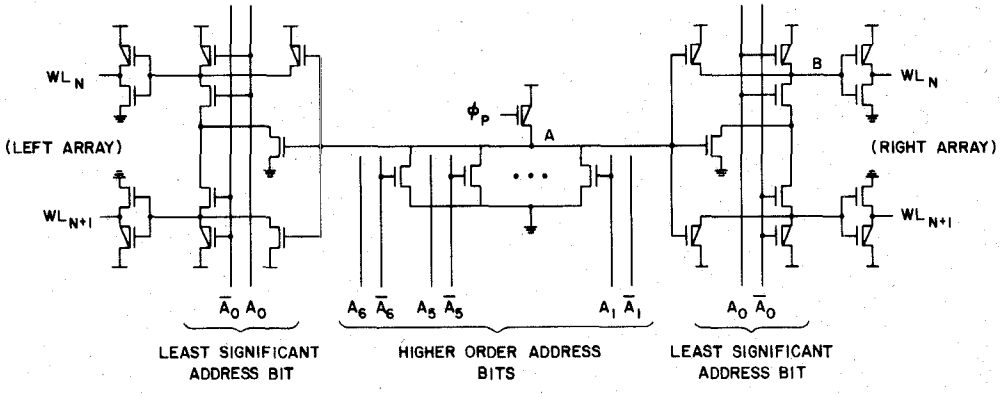


Fig. 8. Row decoder with two stages of decoding.

ity to timing skews is limited to the path through the set signal generator to the sense amp relative to the path through the array to the sense amp. Within these sensitive paths, timing variations due to parameter variations are limited by a number of compensating factors. The use of both p and n devices in the set generator and in the array signal path (n cell access device, p bit switch, p decoupling device) tends to compensate for shifts in p thresholds relative to n thresholds. The use of a double inversion in the set signal generator tends to compensate for shifts in the supply voltages. The relatively small device count in the set generator helps to contain sensitivity to errors between devices of the same type on the same chip. Errors due to on-chip variations in capacitances can be compensated by designing the *FS* line and the ϕ_{SET} line to have capacitance components similar to those of the bit lines.

An SEM of the array and sense-amplifier circuitry is shown in Fig. 7. The set signal generators are at the end of the word lines. As can be seen, the ϕ_{SET} line and *FS* line run the entire length of the array. The sense-amplifier layout is symmetrical and balanced. This layout was generated with the layout-rule-independent physical design tool, and the symmetry was retained as layout rules were changed.

B. Row Decoder

The CMOS row decoder of Fig. 8 is a key block in the access path. It is very fast while also minimizing voltage overshoots and undershoots on the internal nodes of the decoder. Minimization of voltage overshoots and undershoots was a critical factor in the choice of circuits during the design of the 64K CMOS RAM. Conventional CMOS decoder circuits with series connected devices can have internal nodes that may be capacitively coupled well below ground or above the power supply voltage. With this stacked device type of circuit, adjustment of physical design and device sizes to damp the capacitive coupling may result in increased delay for decoder selection. In the decoder circuitry in this design, devices stacked more than two deep were not used. Also, stacking large numbers of devices was avoided elsewhere in the chip. As a consequence of this and other factors, voltage overshoots and undershoots, which could cause charge injection into the substrate and possibly trigger latch-up, were kept to under 0.25 V on all internal nodes of the chip.

The row decoder circuit has two stages of decoding. The first stage is a NOR decoder with the true or complement of the higher order address bits as inputs. The second stage is a two-input NAND decoder with the output of the NOR as

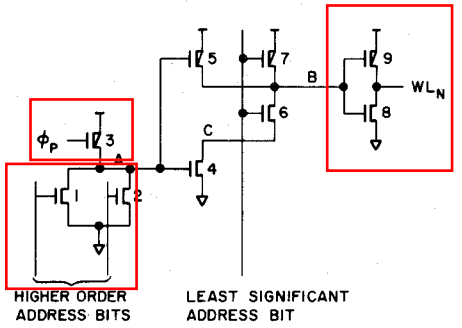


Fig. 9. Simplified row decoder.

one of its inputs and either the true or complement of the least significant address bit (LSB) as the other input. In the 64K CMOS design, since the decoders are in the center of the chip, a single NOR decoder can drive four word lines.

The simplified row decoder circuit of Fig. 9 shows only a single word line to facilitate description of the circuit operation. In standby, all the address lines are low and the output (node A) of the NOR decoder is held to a high voltage through device 3. The word line is in the unselected low state, since the LSB is low, causing the NAND output (node B) to be high. The initiation of an access causes the precharge device 3 to be turned off and the address buffers to drive high either the true or complement of the address inputs to the decoder circuits. A word line is selected only if all the higher order address inputs to its NOR stage remain low and the LSB input to its NAND stage goes high. This results in the NOR decoder output (node A) staying high, the NAND output (node B) going low, and thus the word line going high. Following the selection of a word line and the setting of the sense amps, the selected NOR is discharged due to circuitry not shown on Fig. 8, thereby causing the selected word line to fall. The result is a well-controlled word-line pulsewidth, independent of the cycle time that occurs in an actual application. At the end of an access, all address lines are returned to a low state and the precharge device 3 is turned on. Consequently, the dynamic storage time on the NOR decoder node is small and well controlled.

The word line will remain in the unselected state during an access if the associated LSB remains low or if any of the higher order address inputs go high, causing node A to go low. Unselected word lines, and all word lines during standby, are actively held to ground. However, a momentary bounce on an unselected word line could occur if the NOR output (node A) did not discharge to a low level before the rising LSB turned on device 6 in the NAND stage. Any possibility of an unselected word-line bounce is eliminated by providing two stages of delay of the LSB rising to the higher order address bits rising, as shown in Fig. 10. Address line skew is contained by careful physical placement of the address buffers and address lines, by use of identical layouts for all address buffers, and through design of the address buffer circuit (see Section IV-C). Even with the very conservative bounce protection delay of 0.8 ns, the row decoder is still very fast, with a nominal delay from the higher order address bits rising to the word line rising of only 2.6 ns.

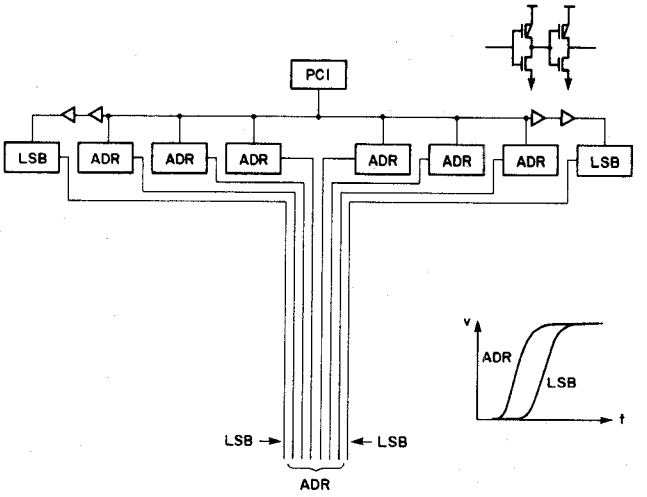


Fig. 10. Delay of least significant address bit from higher order address bits.

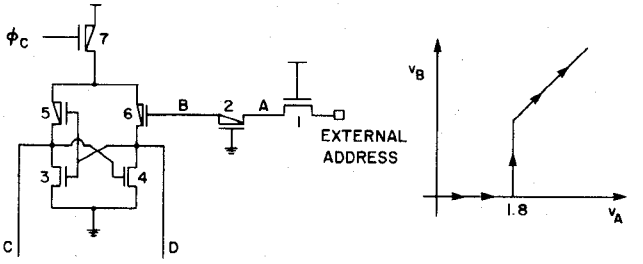


Fig. 11. Simplified input circuit and nonlinear voltage characteristic.

C. Input Circuit

The circuit for input of TTL addresses and data has high speed, low power dissipation, and safe operation. It is shown in a simplified version in Fig. 11, with the complete schematic shown in Fig. 12. Activated by the clock input falling, the circuit converts TTL levels to CMOS on-chip drive, latches the input state, and then disconnects the external input from the internal circuitry during an access. Following an access and the rise of the clock input, the circuit is designed to quickly precharge the internal nodes and the address lines for cycle time minimization. The power dissipation and delay skew as a function of TTL variations and device parameter variations is well contained by this circuit design, which also provides very high speed. The delay through the circuit from the rise of the clock input until the rise of the large capacitance address lines is only 1.9 ns. As will be described in this section, CMOS devices are key to the high-speed safe operation of this circuit—especially as used in the two distinctive portions in Fig. 11: the nonlinear front end and the self-referencing latch.

A salient feature of the high-speed input circuit is the nonlinear front end, which gives the voltage characteristic shown in Fig. 11. Because of the body-effected threshold voltage of p-channel device 2, a solid ground is provided at node B over the full range of low-input TTL signal levels. This can be seen in the voltage characteristic where the voltage at node B versus the voltage at node A is plotted. At the beginning of an access before the clock falls, for

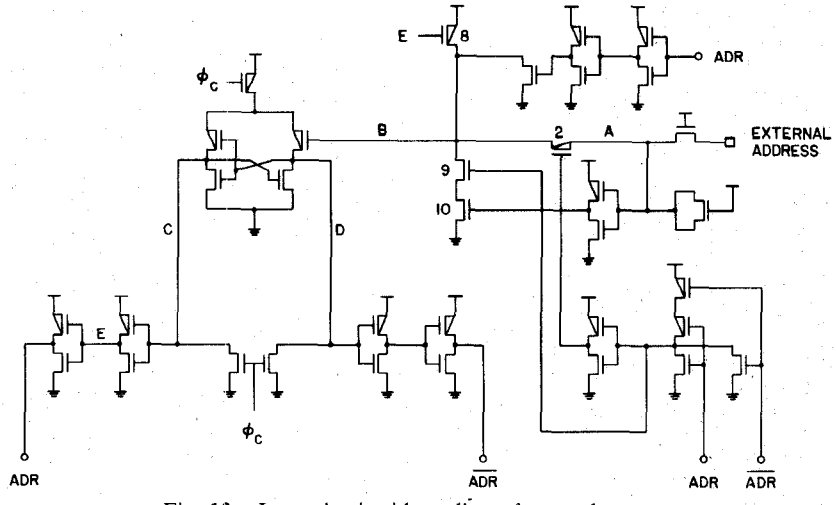


Fig. 12. Input circuit with nonlinear front end.

input voltages less than 1.8 V the input device is cut off and devices 9 and 10, shown on Fig. 12, hold node *B* to ground. Very small devices can be used in the inverter that drives device 10, so that power dissipation due to intermediate voltages on node *A* (input to the inverter) is small. If node *B* is at ground as the clock falls, the latch sets with node *D* high and with no steady-state power dissipation. If the input voltage prior to latch activation is greater than 1.8 V, the small capacitance on node *B* will be quickly charged high through the input devices and the latch will set with node *C* high, causing input device 2 to be turned off and device 8 to be turned on. This will result in a good high being provided on node *B*, thereby cutting off any momentary power dissipation in the latch.

As shown on the complete schematic of the input circuit Fig. 12, the other circuitry driving the devices connected to node *B* served to limit the overshoot and undershoot of nodes to ≤ 0.25 V and isolate the latch during an access, so the address inputs can be set up for the next access. As shown in Fig. 12, the gate of device 2 is switchable, being controlled by the levels of *ADR* and $\overline{ADR}$. At the start of a cycle both *ADR* and $\overline{ADR}$ are low and the gate of device 2 is held at ground. Once the input circuit is activated and the address output becomes valid (*ADR* or $\overline{ADR}$ goes high), the voltage level on the gate of device 2 goes high, turning device 2 off and disconnecting the external input until the latch is reset by the clock rising at the end of an access.

The self-referencing CMOS latch in the input circuit is key to providing high speed, low power, safe operation. Referring to Fig. 11, a balanced physical design is used, so that p-channel devices 5 and 6 are well matched to each other, as are the n-channel latch devices 3 and 4. At the beginning of an access, the clock input is high and nodes *C* and *D* are low, resulting in both devices 3 and 4 being cut off. Shortly, after the beginning of an access, the clock input will fall, turning on p-channel device 7 and charging nodes *C* and *D* until the n-channel latch sets in the direction determined by which of the p-channel steering devices 5 and 6 is most conductive. If node *B* has been charged high through the input devices 1 and 2, p-channel device 5 will be much more conductive than p-channel device 6, steering the setting of the n-channel latch so that node *C* goes high with negligible variation in delay as a function of variation in the TTL high level. If node *B* is low, then initially devices 5 and 6 will be equally conductive. However, as nodes *C* and *D* both begin to charge high, device 5 will quickly become less conductive than device 6, thereby steering the setting of the latch so that node *D* goes high. If the nonlinear front end were not used to provide a good ground at node *B* for any external input voltage less than 1.8 V, then the worst-case TTL low of 0.8 V would result in substantially longer delay through the input circuit relative to the delay for a good TTL high. However, the self-referencing CMOS latch used in conjunction with the nonlinear front end results in good control of delay and power dissipation variations for the full range of TTL input levels, while also providing high-speed operation.

V. Results

The chip has been extensively tested using N^2 test patterns. Functionality has been measured on all 16 data inputs and outputs for a power supply voltage of 3–6 V. The chip is also operational with a ± 10-percent power supply variation over the full range of TTL input levels.

Waveforms showing a $\overline{CS}$ access time of under 15 ns are shown in Fig. 13. The delays for each block in the critical path are given on the block diagram of Fig. 4. Simulations assuming a second level of metal to stitch the word line, 1.0-μm effective channel lengths for the n and p devices, and some minor redesign give a nominal access time of 10 ns.

VI. Physical Design

The use of a ground-rule-independent graphics tool for the high-performance 64K CMOS RAM artwork design is unique. The graphics tool enables timely accommodation

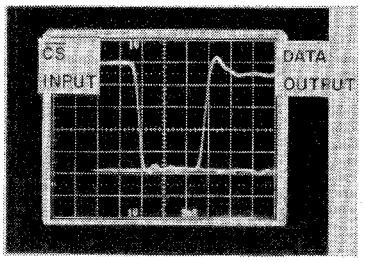


Fig. 13. $\overline{CS}$ access time waveform.

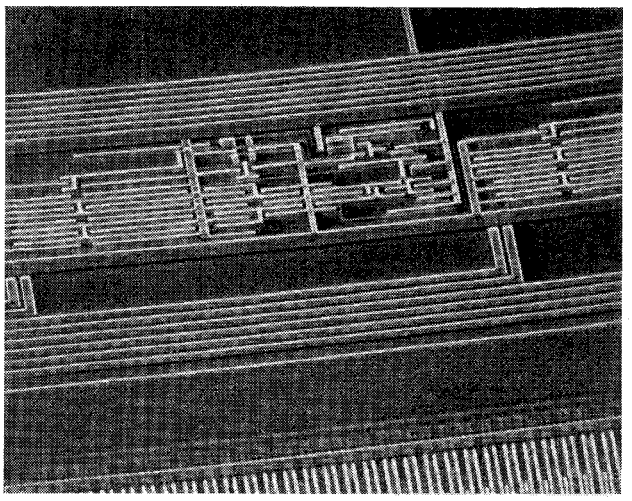
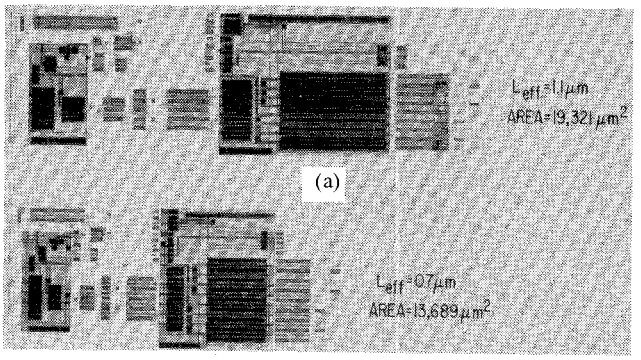


Fig. 14. SEM of row address buffer with nonlinear front end.



(b)

Fig. 15. (a) Plot of address buffer of Fig. 14 which has a minimum effective channel length of 1.1 μm. (b) Plot of same address buffer with the effective channel length being reduced to 0.7 μm along with several other ground rule changes.

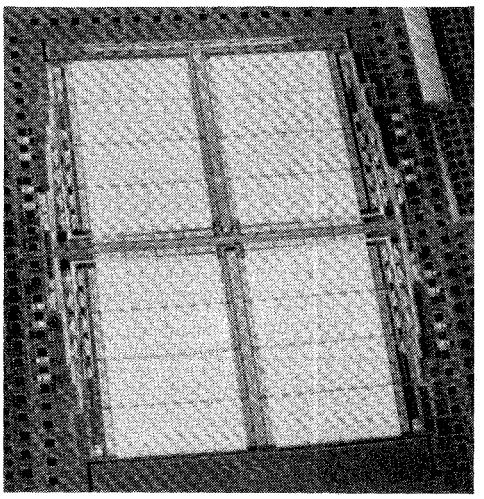


Fig. 16. SEM of the 64K RAM.

of physical layout rule changes during the design cycle. The layout rules are contained in a file which can be changed or updated. Physical layout rule violations are virtually eliminated by the use of this graphics tool. The algorithm used in the approach has been described elsewhere [19].

The artwork for this chip was derived from existing artwork for a chip previously designed using the ground-rule-independent tool. To make this conversion, ~90 percent of the ground rules changed. Roughly six man weeks of time were needed for the conversion. Since the tool was then in an early stage of development, it is felt that this time could be reduced by possibly an order of magnitude. In addition, the tool has been used to generate several versions of the chip for various process development vehicles. The version of the chip described here used the preexisting nonoptimized pad cage used by all versions of the design.

An example will illustrate the potential of the ground-rule-independent layout tool. The SEM of Fig. 14 shows the previously described input circuit used as a row address buffer. The same address buffer shown in Fig. 15(a) has an effective channel length of 1.1 μm and an area of 19321 μm^2. In Fig. 15(b) several ground rules were changed including a change in effective channel length to 0.7 μm. For the same device width-to-length ratios the area reduces to 13689 μm^2. An examination of the aspect ratio of the two plots clearly reveals a more complicated transformation than a simple scaling. The total real time to generate the new graphics data was about 30 s.

An SEM of the 64K CMOS RAM chip is shown in Fig. 16. The chip has a single level of metal. Physically the chip is divided into four 16K quadrants with the row and column decoders in the center. Even with a silicided word line that runs only halfway across the array and a split word-line cell [5], the *RC* delay for a signal propagating down the word line is approximately 3 ns. Each 16K quadrant has four sense amplifiers and data-in buffers located on its periphery.

VII. Summary

A 64K CMOS RAM with an access time of 15 ns has been described. The RAM was built using a single level of metal, an average minimum feature size of 1.35 μm, and an effective channel length of 1.1 and 1.2 μm for n- and p-channel devices, respectively. An access time of 10 ns is possible with the word line stitched on a second level of metal, an effective channel length of 1.0 μm, and some minor redesign. High speed has been achieved through innovative circuits and design concepts. A layout-rule-independent graphics tool was used for the artwork design.

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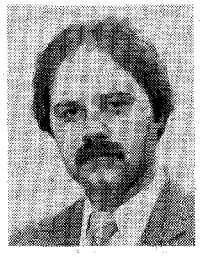

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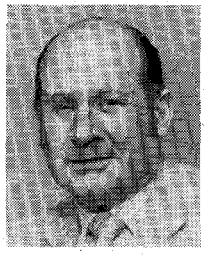

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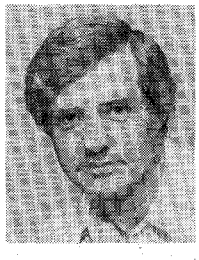

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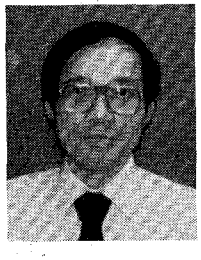

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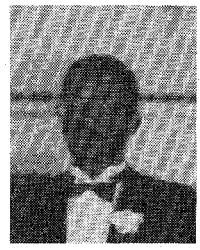

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